Dynamic Analysis of the Negative OFF-State Current in Thin-film Transistors

Wenxing Huo, Rui Zhu, Zengxia Mei, Zuyin Han, Tao Wang, Yanxin Sui, Huili Liang, and Xiaolong Du

***Abstract*— Negative drain currents under positive drain-to-gate voltage were found in the OFF-state transfer curves of thin-film transistors (TFTs). A dynamic model was developed, by accounting for capacitances, to interpret the phenomenon. The capacitor discharging during gate voltage sweeping leads to the negative currents. Test conditions and intrinsic device parameters affect the existence of this phenomenon, which is verified by our experimental results of InGaZnO TFTs.**

***Index Terms*— Dynamic model, thin-film transistors (TFTs).**

I. Introduction

AMORPHOUS oxide semiconductor (AOS)-based thin-film transistor (TFT) is widely investigated in the field of next-generation displays and flexible electronics [1]. Intriguingly, the novel OFF-state current phenomenon of InGaZnO (IGZO) TFTs was found in our previous study [2]. The transfer curves are redrawn in logarithmic [Fig. 1(a)] and linear coordinates [Fig. 1 (b)], respectively. It is found that two minima of the drain current (I_D) appear in the forward gate voltage (V_G) sweeping transfer curve, one close to −7 V and another 0 V, as shown in Fig. 1(a). Fig. 1(b) shows that I_D gradually changes from positive to negative as V_G increases, which occurs around −7 V. I_D will turn back to positive again when V_G reaches the turn-on voltage (0 V here). In the case of logarithmic coordinate [Fig. 1(a)], two minima are naturally seen due to the use of absolute values of I_D, which clearly mark the current polarity conversions. On the other hand, the gate current (I_G) demonstrates opposite polarity to I_D.

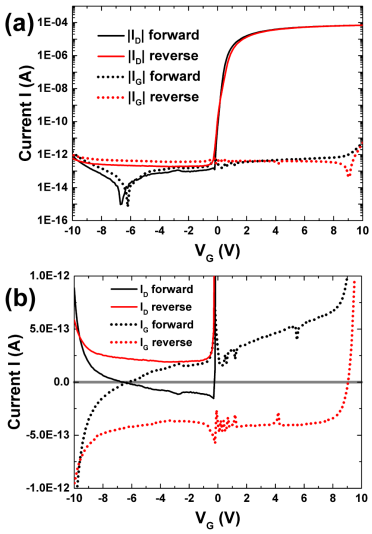

Fig. 1. Novel OFF-state current phenomenon in transfer curves of IGZO TFTs. (a) Logarithmic coordinate. (b) Linear coordinate (data redrawn from [2]).

This phenomenon not only appears in IGZO TFTs but also in ZnO TFTs fabricated on the thin copper substrate [3]. In fact, similar phenomena have been observed in previous publications, as shown in Fig. 2, where the channel materials are oxide [4], organic [5], MoS_2 [6], and nanocrystalline-Si [7]. The OFF-state I_D in Fig. 2(a) and (b) shows the same minima as those in Fig. 1(a). The blank regions with negative V_G in Fig. 2(c) and (d) are the negative currents hidden by the logarithmic coordinate transformations. The positive drain voltage (V_D) and negative V_G in these cases will not lead to negative I_D and positive I_G. This phenomenon exists extensively but seems ignored.

TFT device modeling is helpful for understanding the device physics and optimizing the device performance. Basically, most of the existing models for oxide TFTs focus on the ON-state current [8]–[15]. Jeong and Hong investigated the OFF-current by using ATLAS 2-D device simulator and revealed its dependence on the active layer thickness due to Fermi-level pinning [16]. The off-leakage current of hydrogenated amorphous Si TFTs was attributed to back channel

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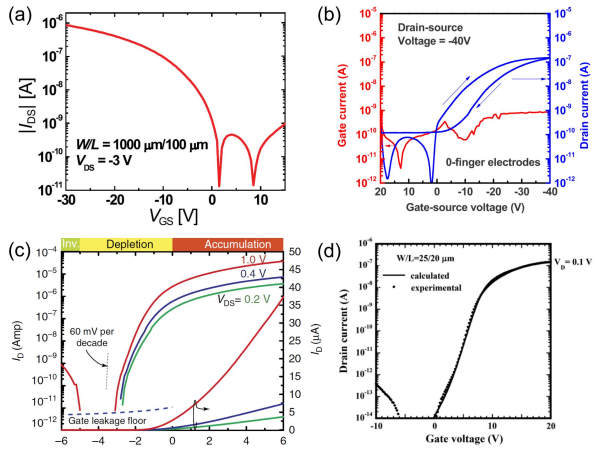

Fig. 2. Similar phenomena in other references. (a) Cu_2O TFT [4]. (b) 6,13-bis(triisopropylsilylethynyl) pentacene organic TFT [5]. (c) Multilayer MoS_2 TFT [6]. (d) Nanocrystalline-Si TFT [7].

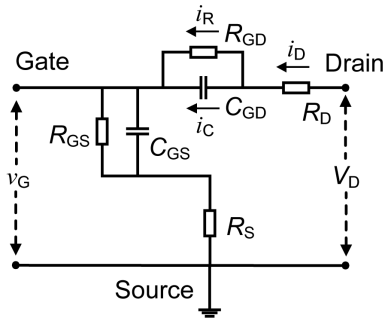

Fig. 3. Dynamic TFT equivalent circuit model in the OFF state.

conduction and Pool−Frenkel emission [17]. However, these static models cannot explain the unusual negative OFF-state drain current. A large-signal dynamic model was developed by accounting for capacitances [18], but it was only applied to the ON-state current. Herein, we develop a dynamic model to explore the mechanism beyond the novel OFF-state current and analyze the affecting factors.

II. Results and Discussion

Although the dynamic ON-state model cannot be obtained by simply adding capacitors between gate and drain–source, it is feasible for the dynamic model to be used in OFF-state condition, as shown in Fig. 3. Note that the bottom-gate staggered TFT structure is used to extract the model, whereas the influence of TFT structure on the negative current phenomenon is negligible. Two nonideal issues are taken into account in the dynamic equivalent circuit model by adding resistances: R_D/R_S for series contact resistance and R_{GD}/R_{GS} for gate insulator leakage. The value of capacitor between gate and drain, C_{GD}, keeps constant in OFF-state at low frequencies [19]. The OFF-state channel current from drain to source for IGZO TFTs (50 yA/μm at 85 °C) [20] is negligible compared to the measurement limit (∼10–17 A for Keithley 4200 with preamplifier). V_D is set to a constant value for transfer curves. The source is grounded. The gate voltage $v_G(t)$ sweeps from a relatively large initial value $v_G(0)$ (negative for forward direction) with a constant rate A (positive for forward direction)

$$v_G(t) = v_G(0) + At. \tag{1}$$

The capacitors are regarded as "open" in the initial state (t= 0), giving initial values of capacitor voltage u_C and capacitor current i_C as

$$u_C(0) = (V_D - v_G(0)) \times \frac{R_{GD}}{R_{GD} + R_D}, \quad i_C(0) = 0. \tag{2}$$

According to Kirchhoff's current law, the dynamic drain current $i_D(t)$ can be described by the sum of the dynamic currents through the gate-to-drain capacitor $i_C(t)$ and resistance $i_R(t)$

$$i_D(t) = i_C(t) + i_R(t) \tag{3}$$

where

$$i_C(t) = C_{GD} \times \frac{du_C(t)}{dt} \tag{4}$$

$$i_R(t) = \frac{u_C(t)}{R_{GD}}. \tag{5}$$

$i_D(t)$ can also be described by

$$i_D(t) = \frac{V_D - u_C(t) - v_G(t)}{R_D}. \tag{6}$$

Substituting (1) and (4)−(6) into (3), we obtained (7) as follows:

$$\frac{V_D - u_C(t) - v_G(0) - At}{R_D} = \frac{u_C(t)}{R_{GD}} + C_{GD} \times \frac{du_C(t)}{dt}. \tag{7}$$

By solving this linear differential equation, the expression of $u_C(t)$ is obtained as follows:

$$u_C(t) = (V_D - v_G(0) - At) \times \frac{R_{GD}}{R_{GD} + R_D} + AR_DC_{GD} \times \left(\frac{R_{GD}}{R_{GD} + R_D}\right)^2 + C_1 \exp\left(-\frac{R_{GD} + R_D}{R_{GD}R_DC_{GD}}t\right) \tag{8}$$

where C_1 is an integration constant. Setting the initial condition in (2), C_1 is calculated as follows:

$$C_1 = -AR_DC_{GD} \times \left(\frac{R_{GD}}{R_{GD} + R_D}\right)^2. \tag{9}$$

Then

$$u_C(t) = (V_D - v_G(0) - At) \times \frac{R_{GD}}{R_{GD} + R_D} + AR_DC_{GD} \times \left(\frac{R_{GD}}{R_{GD} + R_D}\right)^2 \times \left(1 - \exp\left(-\frac{R_{GD} + R_D}{R_{GD}R_DC_{GD}}t\right)\right). \tag{10}$$

Substituting (10) into (6), the expression of $i_D(t)$ is obtained as follows:

$$i_D(t) = \frac{(V_D - v_G(0) - At)}{R_{GD} + R_D} - AC_G \times \left(\frac{R_{GD}}{R_{GD} + R_D}\right)^2 \times \left(1 - \exp\left(-\frac{R_{GD} + R_D}{R_{GD}R_DC_{GD}}t\right)\right). \tag{11}$$

$i_D(t)$ can be regarded as the difference between two items: the former is the current when the capacitor is not considered

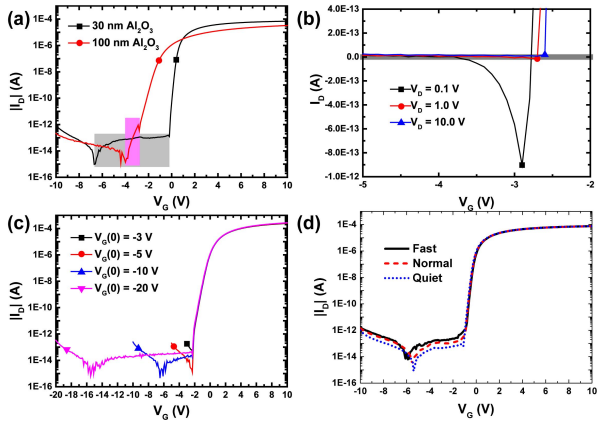

Fig. 4. Verification of the effect of different factors on the OFF-state current. (a) Capacitor C_{GD}. (b) Drain voltage V_D. (c) Initial gate voltage $v_G(0)$. (d) Sweeping rate A.

and the latter is the current caused by capacitor discharging. Since $A > 0$, the latter is positive and increases with t, while the former decreases with t. Therefore, $i_D(t)$ is a decreasing function of t. When the latter is larger than the former, $i_D(t)$ will turn into negative values.

Equation (11) indicates that $i_D(t)$ is affected by many factors, and it is necessary to clarify their individual effect. Generally, $R_D \ll R_{GD}$, (11) could be simplified to

$$i_D(t) = \frac{(V_D - v_G(0) - At)}{R_{GD}} - AC_{GD} \times \left(1 - \exp\left(-\frac{1}{R_D C_{GD}} t\right)\right). \tag{12}$$

There are six factors that can be divided into two categories: test condition parameters V_D, $v_G(0)$, and A; intrinsic device parameters R_{GD}, R_D, and C_{GD}. We choose the value of i_D at a certain time $t = t_1$, then $v_G(t_1) = v_G(0) + At_1$. Eliminating t in (12), i_D is transformed into

$$i_D = \frac{(V_D - v_G(t_1))}{R_{GD}} - AC_{GD} \times \left(1 - \exp\left(-\frac{v_G(t_1) - v_G(0)}{R_D A C_{GD}}\right)\right). \tag{13}$$

Note that all factors are positive except $v_G(0)$. Through simple mathematical analysis, i_D is deduced to monotonically decrease with respect to R_{GD}, C_{GD}, and A, but monotonically increase with respect to R_D, V_D, and $v_G(0)$, respectively. That is, i_D is more likely to turn into negative with larger R_{GD}, C_{GD}, A and smaller R_D, V_D, $v_G(0)$.

Larger R_{GD} and C_{GD} indicate better insulation and fewer dielectric/channel interface defects, while smaller R_D means better contact between drain and channel. Therefore, better TFT parameters are easier to cause the negative OFF-state i_D. That is why, the annealing process affects the OFF-state current of IGZO TFTs on Mica [21]. Annealing eliminates the interface defects and decreases contact resistance, so the negative OFF-state i_D becomes more and more significant as annealing temperature increases. The effect of C_{GD}, V_D, $v_G(0)$, and A can be verified by experiment, as shown in Fig. 4, where the devices are the same with those in [2] except for a thicker Al_2O_3 layer of 100 nm.

First, we verify the effect of C_{GD} by comparing IGZO TFTs with a different thickness of Al_2O_3, as shown in Fig. 4(a). C_{GD} is inversely proportional to dielectric thickness. IGZO TFT with 30-nm Al_2O_3 demonstrates an earlier starting and broader region of negative i_D than that with 100-nm Al_2O_3. Although the thinner dielectric thickness also decreases R_{GD}, the effect may be not be significant as C_{GD}. The effect of V_D on i_D is shown in Fig. 4(b). The transition of i_D to negative values gradually disappears as the drain voltage increases. Fig. 4(c) presents the transfer curves with different $v_G(0)$. As $v_G(0)$ increases from -20 to -3 V, the transition of i_D occurs much later, even disappears. Fig. 4(d) shows the transfer curves with different sweeping rates, which are given by three modes of Keithley 4200: fast with $A = 0.22$ V/s, normal with $A = 0.11$ V/s, and quiet with $A = 0.03$ V/s. The negative i_D in OFF state exhibits an earlier transition and larger absolute values as A increases. The ON-state drain current is independent of the values of $v_G(0)$ or sweeping rates. All these results are consistent with the above conclusion derived.

The ON/OFF ratio is typically extracted from the transfer curve by dividing the maximum with the minimum drain current [1]. However, the existence of negative drain current causes confusion during the extraction. The minimum only represents the polarity conversion and its values almost reach the detection limit. Changes in test conditions can also cause its variations of more than an order of magnitude, as shown in Fig. 4(d). The definition of the ON/OFF ratio should be adopted with great carefulness.

III. Conclusion

We have successfully developed a dynamic model to explain the uncommonly mentioned negative OFF-state drain current in the transfer curve of TFTs. The negative drain current originates from the discharging of gate-to-drain capacitor. The existence of this phenomenon is affected by the contact resistance, gate-to-drain resistance and capacitance, drain voltage, initial gate voltage, and sweeping rates, which is proved by model analysis and experiments. This dynamic model provides a better understanding toward the measurement and analysis of TFTs.

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